

## CLC430

# General Purpose 100MHz Op Amp with Disable

### General Description

The CLC430 is a low cost, wideband monolithic amplifier for general purpose applications. The CLC430 utilizes National's patented current feedback circuit topology to provide an op amp with a slew rate of 2000V/ $\mu$ s, 100MHz unity-gain bandwidth and fast output disable function. Like all current feedback op amps, the CLC430 allows the frequency response to be optimized (or adjusted) by the selection of the feedback resistor. For demanding video applications, the 0.1dB bandwidth to 20MHz and differential gain/phase of 0.03%/0.05° make the CLC430 the preferred component for broadcast quality NTSC and PAL video systems.

The large voltage swing (28V<sub>PP</sub>), continuous output current (85mA) and slew rate (2000V/ $\mu$ s) provide high-fidelity signal conditioning for applications such as CCDs, transmission lines and low impedance circuits. Even driving loads of 100 $\Omega$ , the CLC430 provides very low 2nd and 3rd harmonic distortion at 1MHz (-76/-82dBc).

Video distribution, multimedia and general purpose applications will benefit from the CLC430's wide bandwidth and disable feature. Power is reduced and the output becomes a high impedance when disabled. The wide gain range of the CLC430 makes this general purpose op amp an improved solution for circuits such as active filters, differential-to-single-ended drivers, DAC transimpedance amplifiers and MOSFET drivers.

### Features

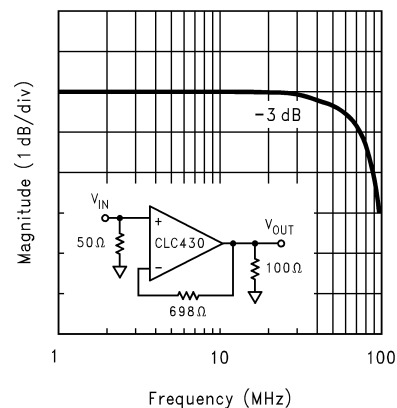
- 0.1dB gain flatness to 20MHz ( $A_V = +2$ )
- 100MHz bandwidth ( $A_V = +1$ )
- 2000V/ $\mu$ s slew rate

- 0.03%/0.05° differential gain/phase
- $\pm 5V$ ,  $\pm 15V$  or single supplies
- 100ns disable to high impedance output
- Wide gain range
- Low cost

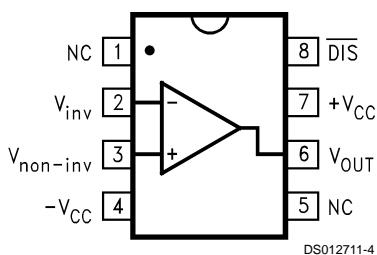
### Applications

- Video distribution
- CCD clock driver
- Multimedia systems
- DAC output buffers
- Imaging systems

Unity-Gain Frequency Response

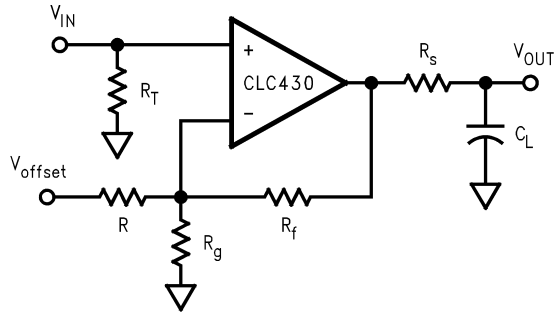


### Connection Diagram

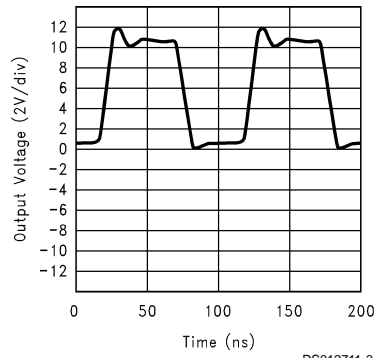


Pinout  
DIP & SOIC

### Typical Application



DS012711-2



CCD Clock Driver

### Ordering Information

| Package            | Temperature Range<br>Industrial | Part Number | Packaging<br>Marking | NSC<br>Drawing |
|--------------------|---------------------------------|-------------|----------------------|----------------|
| 8-pin plastic DIP  | -40°C to +85°C                  | CLC430AJP   | CLC430AJP            | N08E           |
| 8-pin plastic SOIC | -40°C to +85°C                  | CLC430AJE   | CLC430AJE            | M08A           |

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                              |                  |
|------------------------------|------------------|
| Supply Voltage               | ±16.5V           |
| Short Circuit Current        | (see note 4)     |
| Common-Mode Input Voltage    | ±V <sub>CC</sub> |
| Maximum Junction Temperature | +150°C           |
| Storage Temperature Range    | -65°C to +150°C  |

Lead Temperature (soldering 10 sec)  
ESD (human body model)

+300°C  
4000V

**Operating Ratings**

|                    |               |               |
|--------------------|---------------|---------------|
| Thermal Resistance |               |               |
| Package            | $\theta_{JC}$ | $\theta_{JA}$ |
| MDIP               | 60°C/W        | 115°C/W       |
| SOIC               | 55°C/W        | 135°C/W       |

**Electrical Characteristics**

V<sub>CC</sub> = ±15 V, A<sub>V</sub> = +2V/V, R<sub>f</sub> = 604Ω, R<sub>L</sub> = 100Ω; unless specified

| Symbol                               | Parameter                         | Conditions                                     | V <sub>CC</sub> | Typ   | Min/Max Ratings (Note 2) |           |             | Units  |
|--------------------------------------|-----------------------------------|------------------------------------------------|-----------------|-------|--------------------------|-----------|-------------|--------|
|                                      | Ambient Temperature               | CLC430AJ                                       |                 | +25°C | +25°C                    | 0 to 70°C | -40 to 85°C |        |
| <b>Frequency Domain Response</b>     |                                   |                                                |                 |       |                          |           |             |        |
|                                      | Unity-Gain Bandwidth              | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          | ±15             | 100   |                          |           |             | MHz    |
|                                      | Small-Signal Bandwidth            | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          | ±15             | 75    | 50                       | 45        | 42          | MHz    |
|                                      |                                   | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          | ±5              | 55    | 35                       |           |             | MHz    |
|                                      | 0.1dB Bandwidth                   | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          | ±15             | 20    | 7                        |           |             | MHz    |
|                                      |                                   | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          | ±5              | 16    |                          |           |             | MHz    |
|                                      | Large-Signal Bandwidth            | V <sub>OUT</sub> < 10V <sub>PP</sub>           |                 | 30    | 22                       | 20        | 19          | MHz    |
|                                      | Gain Flatness                     | V <sub>OUT</sub> < 1.0V <sub>PP</sub>          |                 |       |                          |           |             |        |
|                                      | Peaking                           | DC to 10MHz                                    |                 | 0.0   | 0.1                      | 0.2       | 0.2         | dB     |
|                                      | Rolloff                           | DC to 20MHz                                    |                 | 0.1   | 0.7                      | 1.0       | 1.2         | dB     |
|                                      | Linear Phase Deviation            | DC to 20MHz                                    |                 | 0.5   | 1.8                      | 2.0       | 2.1         | deg    |
|                                      | Differential Gain                 | 4.43 MHz, R <sub>L</sub> = 150Ω                | ±15             | 0.03  | 0.05                     | 0.06      | 0.06        | %      |
|                                      |                                   | 4.43 MHz, R <sub>L</sub> = 150Ω                | ±5              | 0.03  | 0.05                     |           |             | %      |
|                                      | Differential Phase                | 4.43 MHz, R <sub>L</sub> = 150Ω                | ±15             | 0.05  | 0.09                     | 0.12      | 0.13        | deg    |
|                                      |                                   | 4.43 MHz, R <sub>L</sub> = 150Ω                | ±5              | 0.09  | 0.19                     |           |             | deg    |
| <b>Time Domain Response</b>          |                                   |                                                |                 |       |                          |           |             |        |
|                                      | Rise and Fall Time                | 2V Step                                        |                 | 5     | 7                        | 7         | 7           | ns     |
|                                      |                                   | 10V Step                                       |                 |       | 10                       | 14        | 14          | 14     |
|                                      | Settling Time to 0.05%            | 2V Step                                        |                 | 35    | 50                       | 55        | 55          | ns     |
|                                      | Overshoot                         | 2V Step                                        |                 | 5     | 15                       | 15        | 15          | %      |
|                                      | Slew Rate                         | 20V Step                                       |                 | 2000  | 1500                     | 1450      | 1450        | V/μs   |
| <b>Distortion And Noise Response</b> |                                   |                                                |                 |       |                          |           |             |        |
|                                      | 2nd Harmonic Distortion           | 1V <sub>PP</sub> , 1MHz, R <sub>L</sub> = 500Ω |                 | -89   |                          |           |             | dBc    |
|                                      | 3rd Harmonic Distortion           | 1V <sub>PP</sub> , 1MHz, R <sub>L</sub> = 500Ω |                 | -92   |                          |           |             | dBc    |
|                                      | Input Voltage Noise               | >1MHz                                          |                 | 3.0   | 3.5                      | 3.7       | 3.8         | nV/√Hz |
|                                      | Non-Inverting Input Current Noise | >1MHz                                          |                 | 3.2   | 6.0                      | 6.3       | 6.8         | pA/√Hz |
|                                      | Inverting Input Current Noise     | > 1MHz                                         |                 | 15    | 18                       | 20        | 21          | pA/√Hz |
| <b>DC Performance</b>                |                                   |                                                |                 |       |                          |           |             |        |
|                                      | Input Offset Voltage (Note 3)     |                                                | ±15             | 1.0   | 7.5                      | 9.0       | 10.0        | mV     |
|                                      | Average Drift                     |                                                |                 | 25    | -                        | 50        | 50          | μV/°C  |
|                                      | Input Bias Current (Note 3)       | Non-Inverting                                  | ±15, ±5         | 3     | 14                       | 16        | 20          | μA     |
|                                      | Average Drift                     |                                                | -               | 10    | -                        | 100       | 100         | nA/°C  |

## Electrical Characteristics (Continued)

$V_{CC} = \pm 15\text{ V}$ ,  $A_V = +2\text{V/V}$ ,  $R_f = 604\Omega$ ,  $R_L = 100\Omega$ ; unless specified

| Symbol                           | Parameter                       | Conditions     | $V_{CC}$              | Typ        | Min/Max Ratings (Note 2) |            |            |           | Units                      |
|----------------------------------|---------------------------------|----------------|-----------------------|------------|--------------------------|------------|------------|-----------|----------------------------|
| <b>DC Performance</b>            |                                 |                |                       |            |                          |            |            |           |                            |
|                                  | Input Bias Current (Note 3)     | Inverting      | $\pm 15$ ,<br>$\pm 5$ | 3          | 14                       | 15         | 17         |           | $\mu\text{A}$              |
|                                  | average drift                   |                | -                     | 10         | -                        | 60         | 90         |           | $\text{nA}/^\circ\text{C}$ |
|                                  | Power-Supply Rejection Ratio    | DC             |                       | 62         | 56                       | 54         | 53         |           | dB                         |
|                                  | Common-Mode Rejection Ratio     | DC             |                       | 62         | 54                       | 53         | 52         |           | dB                         |
|                                  | Supply Current (Note 3)         | $R_L = \infty$ | $\pm 15$ ,<br>$\pm 5$ | 11, 8.5    | 12                       | 13         | 14.5       |           | mA                         |
|                                  | Disabled (Note 3)               | $R_L = \infty$ | $\pm 15$ ,<br>$\pm 5$ | 1.5        | 2.0                      | 2.2        | 2.4        |           | mA                         |
| <b>Switching Performance</b>     |                                 |                |                       |            |                          |            |            |           |                            |
|                                  | Turn On Time                    |                |                       | 200        | 300                      | 320        | 340        |           | ns                         |
|                                  | Turn Off Time                   | (Note 5)       |                       | 100        | 200                      | 200        | 200        |           | ns                         |
|                                  | Off Isolation                   | 10MHz          |                       | 59         | 56                       | 56         | 56         |           | dB                         |
|                                  | High Input Voltage              | $V_{IH}$       | $\pm 15$              | 11.8       | 12.5                     | 12.7       |            |           | V                          |
|                                  |                                 |                | $\pm 5$               | 1.8        | 2.5                      | 2.7        |            |           | V                          |
|                                  | Low Input Voltage               | $V_{IL}$       | $\pm 15$              | 10.8       | 10.5                     | 10.0       |            |           | V                          |
|                                  |                                 |                | $\pm 5$               | 0.8        | 0.6                      | 0.1        |            |           | V                          |
| <b>Miscellaneous Performance</b> |                                 |                |                       |            |                          |            |            |           |                            |
|                                  | Non-Inverting Input Resistance  |                |                       | 8.0        | 3.0                      | 2.5        | 1.7        |           | $\text{M}\Omega$           |
|                                  | Non-Inverting Input Capacitance |                |                       | 0.5        | 1.0                      | 1.0        | 1.0        |           | pF                         |
|                                  | Input Voltage Range             | Common Mode    | $\pm 5$               | $\pm 12.5$ | $\pm 12.3$               | $\pm 12.1$ | $\pm 11.8$ |           | V                          |
|                                  |                                 | Common Mode    |                       | $\pm 5$    | $\pm 2.5$                | $\pm 2.3$  | $\pm 2.2$  | $\pm 1.9$ |                            |
|                                  | Output Voltage Range            | $R_L = \infty$ | $\pm 15$              | $\pm 14$   | $\pm 13.7$               | $\pm 13.7$ | $\pm 13.6$ |           | V                          |
|                                  |                                 | $R_L = \infty$ |                       | $\pm 5$    | $\pm 4.0$                | $\pm 3.9$  | $\pm 3.8$  | $\pm 3.7$ |                            |
|                                  | Output Current                  |                |                       | $\pm 85$   | $\pm 60$                 | $\pm 50$   | $\pm 45$   |           | mA                         |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

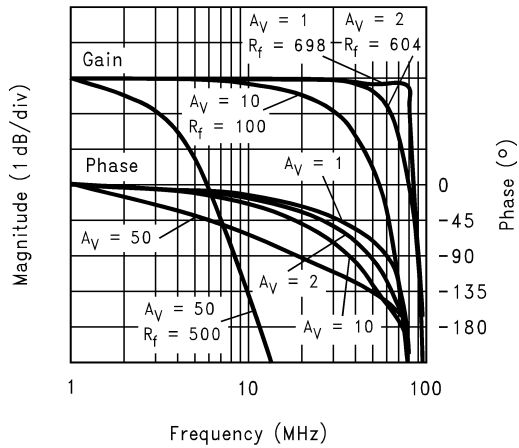
**Note 3:** AJ-level: spec. is 100% tested at  $+25^\circ\text{C}$ .

**Note 4:** Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 125mA.

**Note 5:** To  $<50\text{dB}$  attenuation @10MHz.

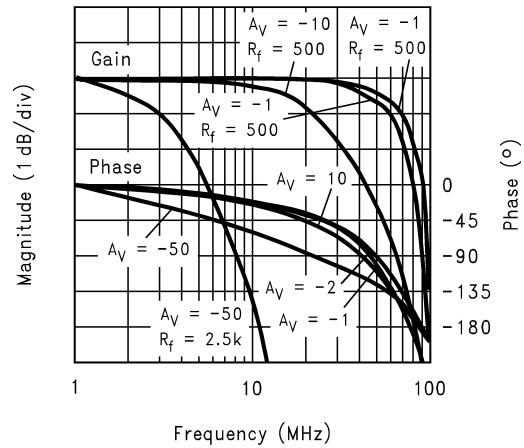
**Typical Performance Characteristics** ( $V_{CC} = \pm 15V$ ,  $A_V = +2V/V$ ,  $R_f = 640\Omega$ ,  $R_L = 100\Omega$ ; Unless Specified)

**Non-Inverting Frequency Response**



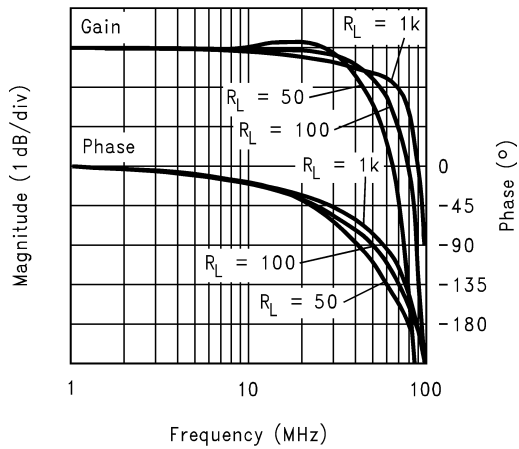
DS012711-6

**Inverting Frequency Response**



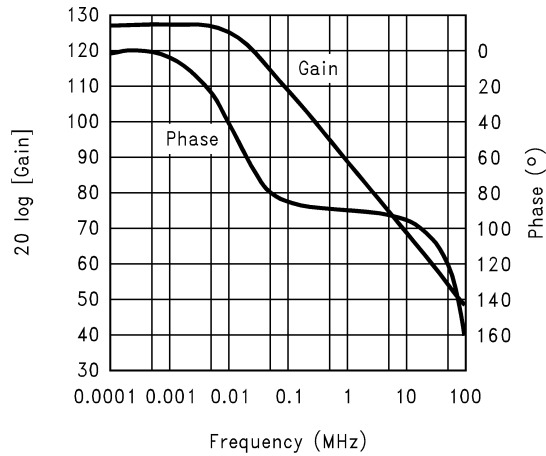
DS012711-7

**Frequency Response vs. Load**



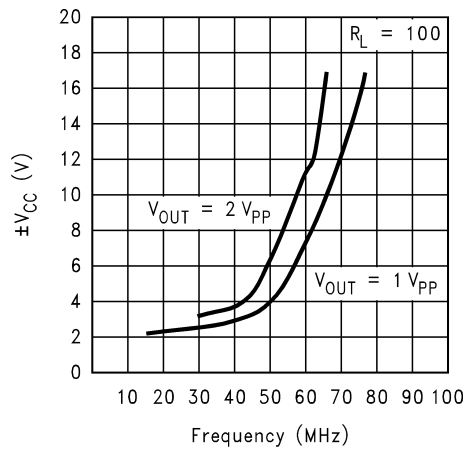
DS012711-8

**Open-Loop Transimpedance Gain, Z(s)**



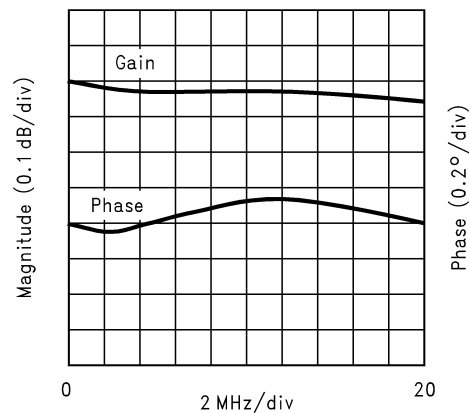
DS012711-9

**-3dB Bandwidth vs.  $V_{CC}$**



DS012711-10

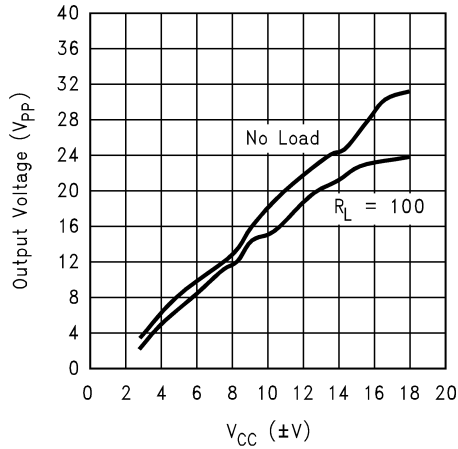
**Gain Flatness and Linear Phase**



DS012711-11

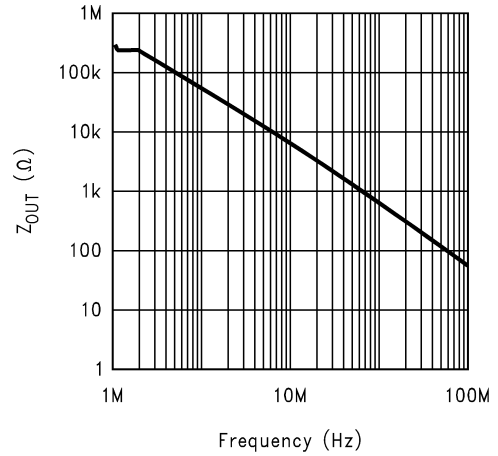
**Typical Performance Characteristics** ( $V_{CC} = \pm 15V$ ,  $A_V = +2V/V$ ,  $R_f = 640\Omega$ ,  $R_L = 100\Omega$ ; Unless Specified)) (Continued)

**Maximum Output Voltage vs.  $V_{CC}$**



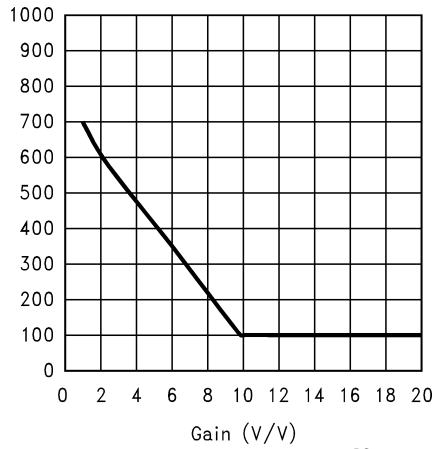
DS012711-12

**Output Impedance, Disable Mode**



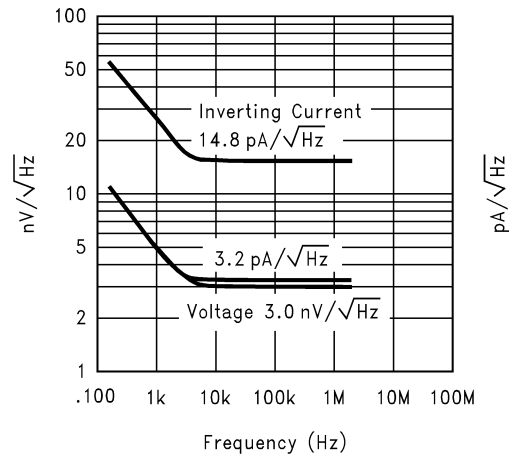
DS012711-13

**Recommended  $R_f$  vs. Gain**



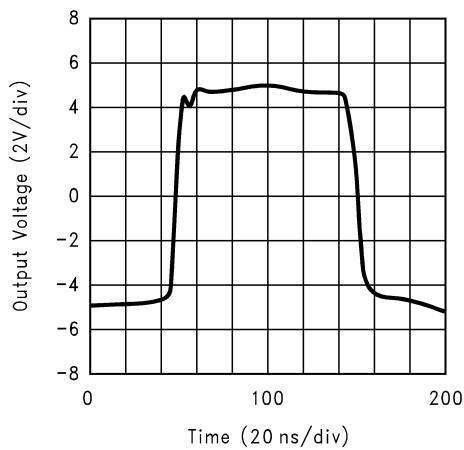
DS012711-14

**Equivalent Input Noise**



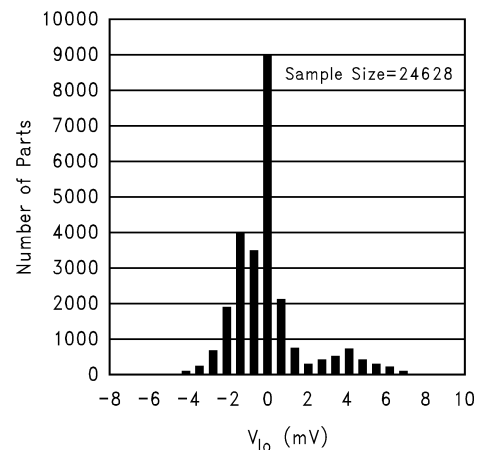
DS012711-15

**Large Signal Pulse Response**



DS012711-16

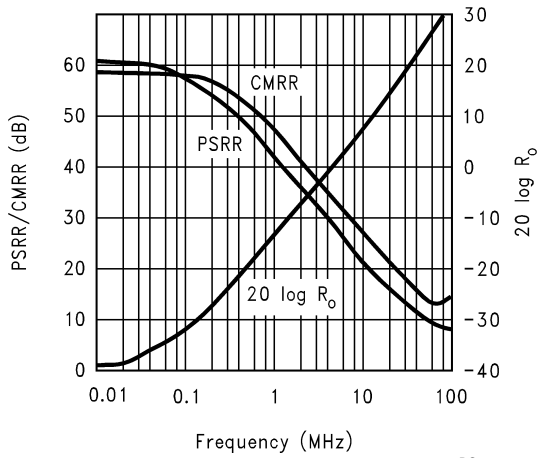
**Histogram of Input Offset Voltage**



DS012711-17

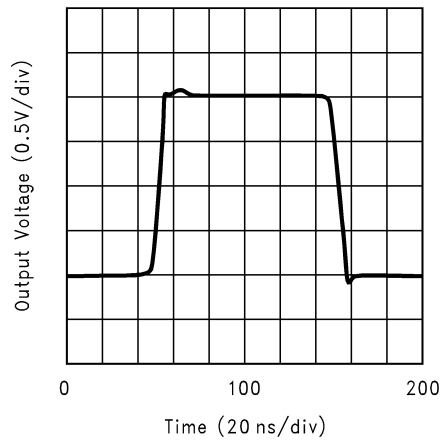
**Typical Performance Characteristics** ( $V_{CC} = \pm 15V$ ,  $A_V = +2V/V$ ,  $R_f = 640\Omega$ ,  $R_L = 100\Omega$ ; Unless Specified)) (Continued)

**PSRR, CMRR and Closed Loop  $R_o$**



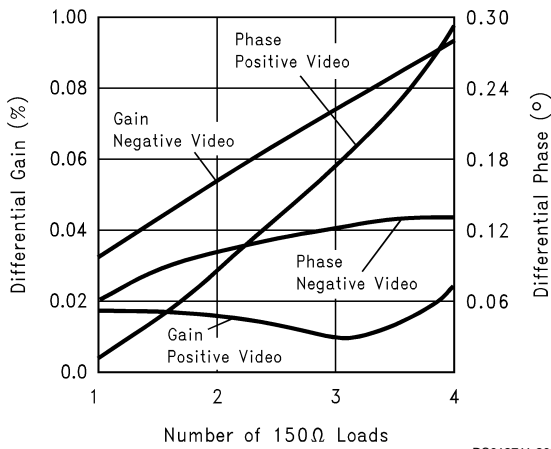
DS012711-18

**Small Signal Pulse Response**



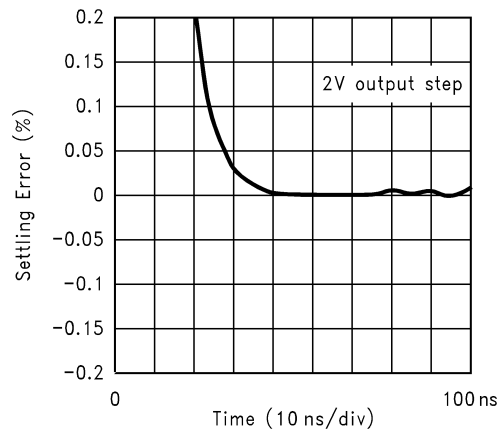
DS012711-19

**Differential Gain and Phase (3.58MHz)**



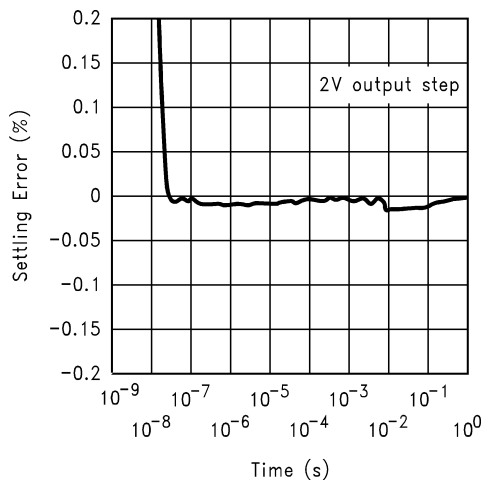
DS012711-20

**Short Term Settling Time**



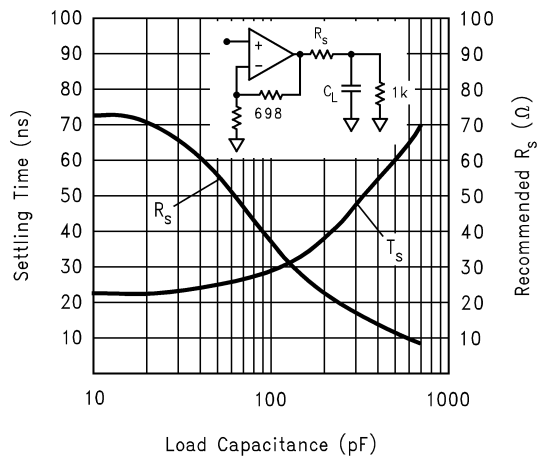
DS012711-21

**Long Term Settling Time**



DS012711-22

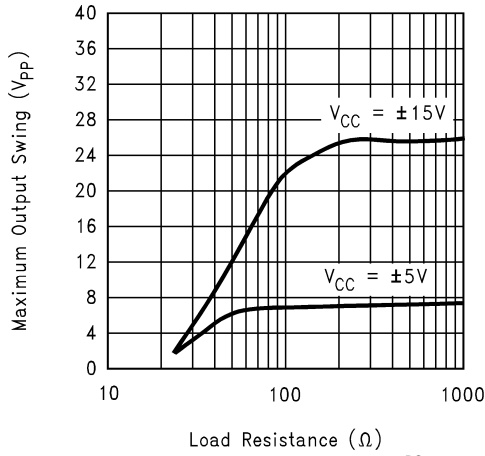
**Settling Time vs. Capacitive Load**



DS012711-23

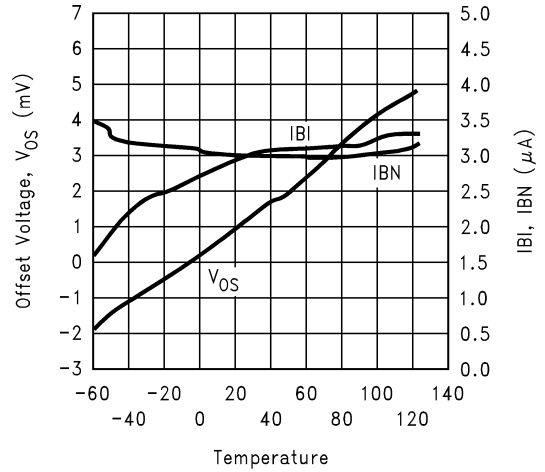
**Typical Performance Characteristics** ( $V_{CC} = \pm 15V$ ,  $A_V = +2V/V$ ,  $R_f = 640\Omega$ ,  $R_L = 100\Omega$ ; Unless Specified)) (Continued)

**Output Voltage Swing vs. Load Resistance**



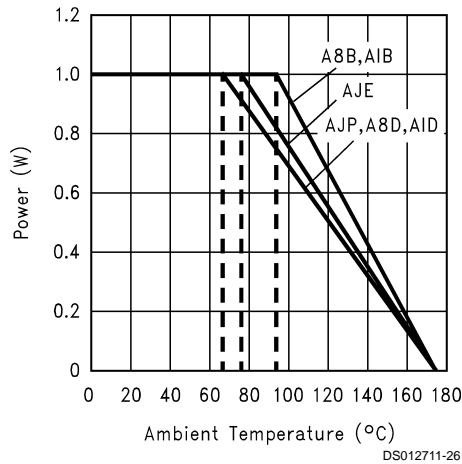
DS012711-24

**Typical IBI, IBN, VOS vs. Temperature**



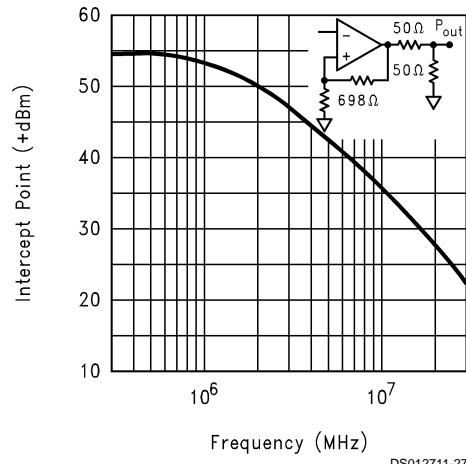
DS012711-25

**Power Derating Curves**



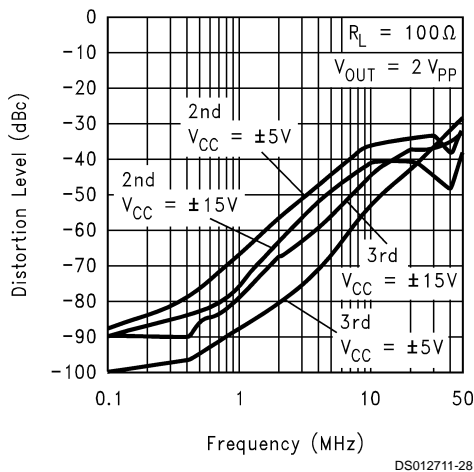
DS012711-26

**2-Tone, 3rd Order Intermodulation Intercept**



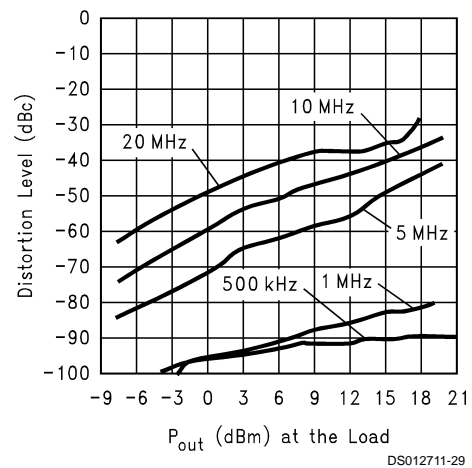
DS012711-27

**Harmonic Distortion vs. Frequency**



DS012711-28

**3rd Harmonic Distortion vs. P<sub>OUT</sub>**

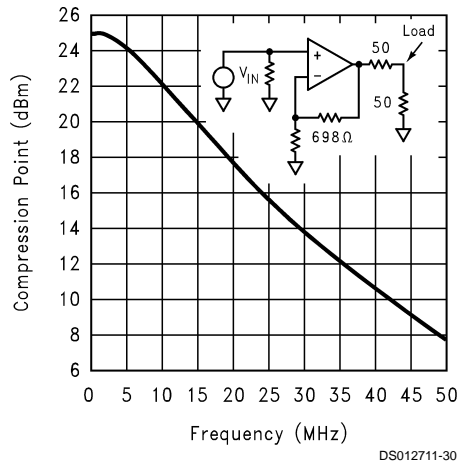


DS012711-29

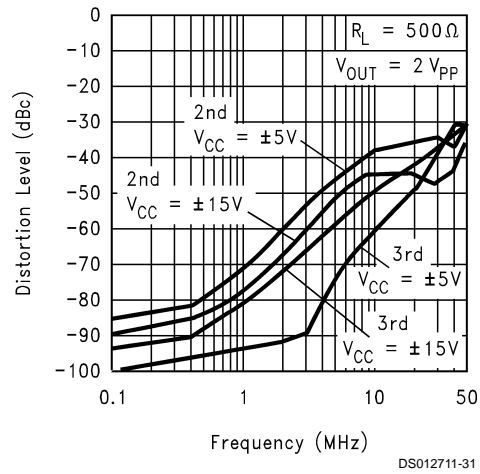


**Typical Performance Characteristics** ( $V_{CC} = \pm 15V$ ,  $A_V = +2V/V$ ,  $R_f = 640\Omega$ ,  $R_L = 100\Omega$ ; Unless Specified)) (Continued)

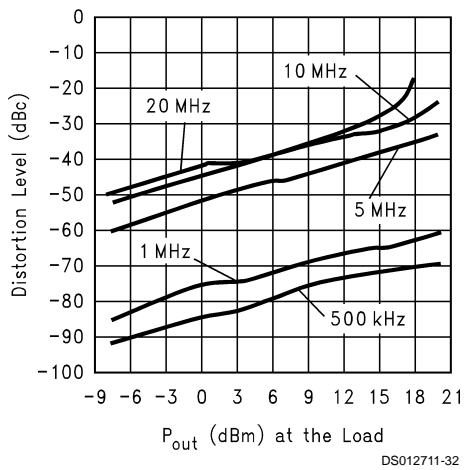
**-1dB Compression to Load**



**Harmonic Distortion vs. Frequency**



**2nd Harmonic Distortion vs.  $P_{OUT}$**



## Application Division

### General Design Considerations

The CLC430 is a general purpose current-feedback amplifier for use in a variety of small and large signal applications. Use the feedback resistor to fine tune the gain flatness and -3dB bandwidth for any gain setting. National provides information for the performance at a gain of +2 for small and large signal bandwidths. The plots show feedback resistor values for selected gains.

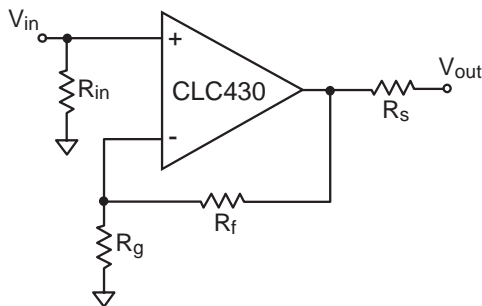
### Gain

Use the following equations to set the CLC430's non-inverting or inverting gain:

$$\text{Non-Inverting Gain} = 1 + \frac{R_f}{R_g}$$

$$\text{Inverting Gain} = -\frac{R_f}{R_g}$$

Choose the resistor values for non-inverting or inverting gain by the following steps.



DS012711-34

FIGURE 1. Component Identification

- 1) Select the recommended feedback resistor  $R_f$  (refer to plot in the plot section entitled  $R_f$  vs. Gain).
- 2) Choose the value of  $R_g$  to set gain.
- 3) Select  $R_s$  to set the circuit output impedance.
- 4) Select  $R_{in}$  for input impedance and input bias.

### High Gains

Current feedback closed-loop bandwidth is independent of gain-bandwidth-product for small gain changes. For larger gain changes the optimum feedback resistor  $R_f$  is derived by the following:

$$R_f = 724\Omega - 60\Omega \times (A_v).$$

As gain is increased, the feedback resistor allows bandwidth to be held constant over a wide gain range. For a more complete explanation refer to application note OA-25 Stability Analysis of Current-Feedback Amplifiers.

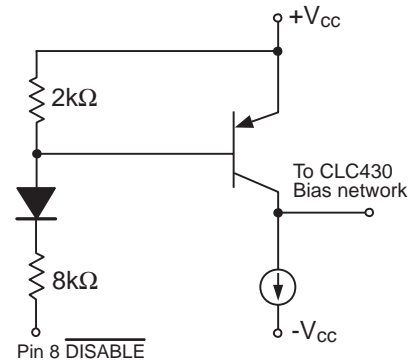
Resistors have varying parasitics that affect circuit performance in high speed design. For best results, use leaded metal-film resistors or surface mount resistors. A SPICE model for the CLC430 is available to simulate overall circuit performance.

### Enable/Disable Function

The CLC430 amplifier features an enable/disable function that changes the output and inverting input from low to high impedance. The pin 8 enable/disable logic levels are as follows:

|          |           |          |
|----------|-----------|----------|
| $V_{CC}$ | $\pm 15V$ | $\pm 5V$ |
| Enable   | $> 12.7V$ | $> 2.7V$ |
| Disable  | $< 10.0V$ | $< 0.08$ |

The amplifier is enabled with pin 8 left open due to the 2k $\Omega$  pull-up resistor, shown in Figure 2.

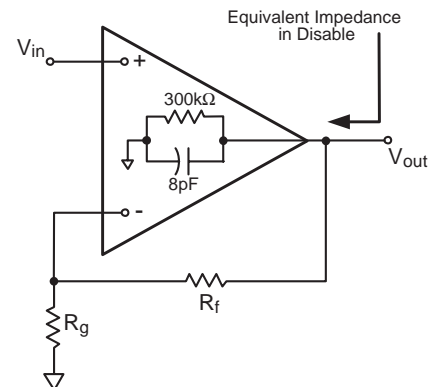


DS012711-35

FIGURE 2. Pin 8 Equivalent Disable Circuit

Open-collector or CMOS interfaces are recommended to drive pin 8. The turn on and off time depends on the speed of the digital interface.

The equivalent output impedance when disabled is shown in Figure 3. With  $R_g$  connected to ground, the sum of  $R_f$  and  $R_g$  dominates and reduces the disabled output impedance. To raise the output impedance in the disabled state, connect the CLC430 as a unity-gain voltage follower by removing  $R_g$ . Current-feedback op-amps need the recommended  $R_f$  in a unity-gain follower circuit. For high density circuit layouts consider using the dual CLC431 (with disable) or the dual CLC432 (without disable).



DS012711-36

FIGURE 3. Equivalent Disabled Output Impedance

### 2nd and 3rd Harmonic Distortion

To meet low distortion requirements, recognize the effect of the feedback resistor. Increasing the feedback resistor will decrease the loop gain and increase distortion. Decreasing the load impedance increases 3rd harmonic distortion more than 2nd.

## Application Division (Continued)

### Differential Gain and Differential Phase

The CLC430 has low DG and DP errors for video applications. Add an external pulldown resistor to the CLC430's output to improve DG and DP as seen in *Figure 4*. A 604Ω  $R_p$  will improve DG and DP to 0.01% and 0.02°.

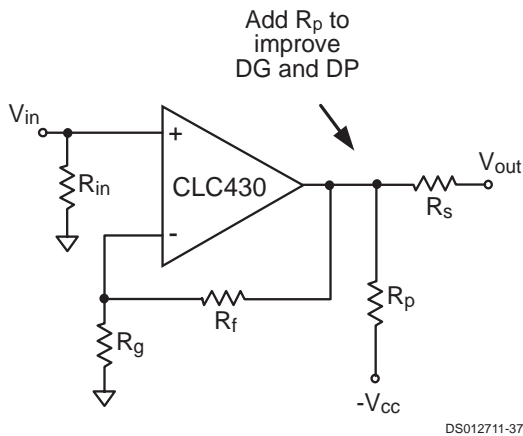


FIGURE 4. Improved DG and DP Video Amplifier

### Printed Circuit Layout

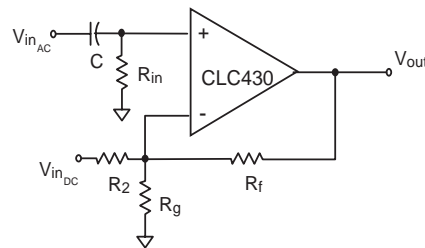
To get the best amplifier performance careful placement of the amplifier, components and printed circuit traces must be observed. Place the 0.1μF ceramic decoupling capacitors less than 0.1" (3mm) from the power supply pins. Place the 6.8μF tantalum capacitors less than 0.75" (20mm) from the power supply pins. Shorten traces between the inverting pin and components to less than 0.25" (6mm). Clear ground plane 0.1" (3mm) away from pads and traces that connect to the inverting, non-inverting and output pins. Do not place ground or power plane beneath the op-amp package. National provides literature and evaluation boards 730013 DIP or 730027 SOIC illustrating the recommended op-amp layout.

### Applications Circuits

#### Level Shifting

The circuit shown in *Figure 5* implements level shifting by AC coupling the input signal and summing a DC voltage. The resistor  $R_{in}$  and the capacitor  $C$  set the high-pass break frequency. The amplifier closed-loop bandwidth is fixed by the selection of  $R_f$ . The DC and AC gains for circuit of *Figure 5* are different. The AC gain is set by the ratio of  $R_f$  and  $R_g$ . And the DC gain is set by the parallel combination of  $R_g$  and  $R_2$ .

$$V_{out} = V_{in_{ac}} \left( 1 + \left( \frac{R_f}{R_g \parallel R_2} \right) \right) - V_{in_{dc}} \left( \frac{R_f}{R_2} \right)$$

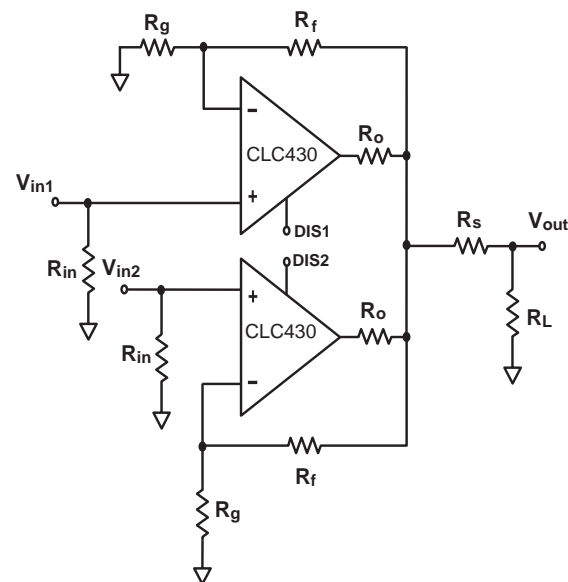


DS012711-38

FIGURE 5. Level Shifting Circuit

#### Multiplexing

Multiple signal switching is easily handled with the disable function of the CLC430. Board trace capacitance at the output pin will affect the frequency response and switching transients. To lessen the effects of output capacitance place a resistor ( $R_o$ ) within the feedback loop to isolate the outputs as shown in *Figure 6*. To match the mux output impedance to a transmission line, add a resistor ( $R_s$ ) in series with the output.



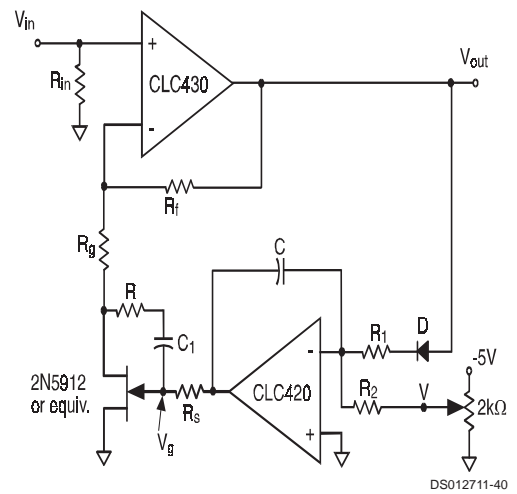
DS012711-39

FIGURE 6. Output Connection

## Application Division (Continued)

### Automatic Gain Control

Current-feedback amplifiers can implement very fast automatic-gain control circuits. The circuit shown in *Figure 7* shows an AGC circuit using the CLC430, a half-wave rectifier, an integrator and a FET. The CLC430 current-feedback amplifier maintains constant bandwidth and linear phase over AGC's gain range. This circuit effectively controls the output level for continuous signals.



**FIGURE 7. AGC Circuit**

The bandwidth of CLC430 AGC is limited by  $R_f$ , the feedback resistor. The FET gate voltage is limited to a range of:

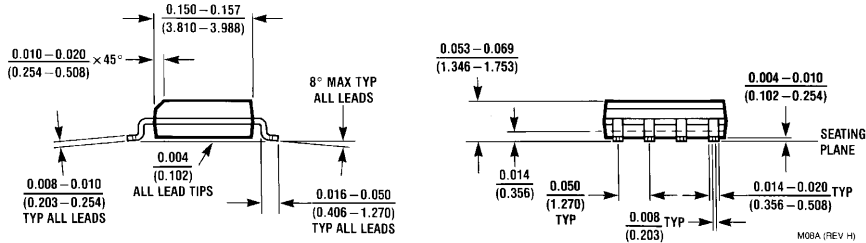
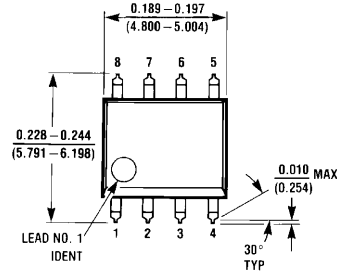
$$-2.5 < V_g < -1$$

$R$  of  $750\Omega$  and  $C_1$  of  $1.0\mu\text{F}$  gives a useful  $R_{ds}$  range of approximately  $150$  to  $2\text{k}\Omega$ . Scaling the integrator gain or adding attenuation before the diode  $D$  accommodates large signal swings. Determine the overall gain by:

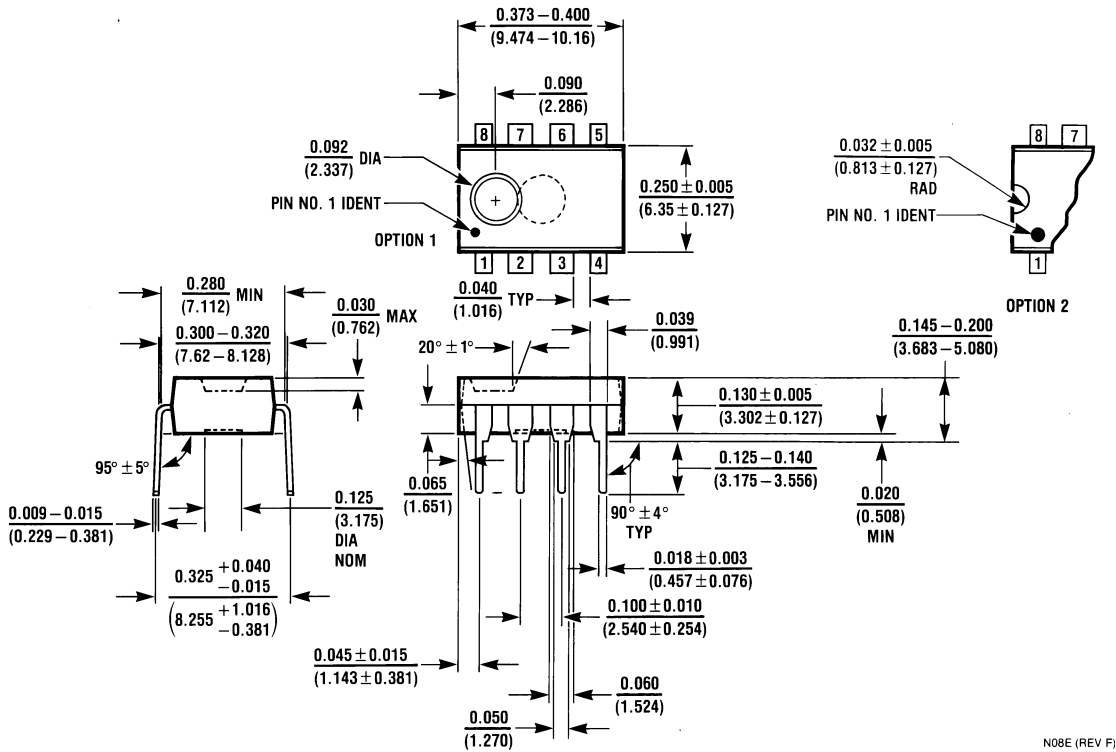
$$1 + \frac{R_f}{R_g + R_{ds}}$$

The integrator sets the loop time constant.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**8-Pin SOIC**  
**NS Package Number M08A**



**8-Pin MDIP**  
**NS Product Number N08E**

## Notes

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com  
www.national.com

**National Semiconductor Europe**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507